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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,902	08/21/2003	Cheng-Ming Yih	4425-315	6430
7590	01/21/2005			EXAMINER HO, TU TU V
LOWE HAUPTMAN GILMAN & BERNER, LLP Suite 310 1700 Diagonal Road Alexandria, VA 22314			ART UNIT 2818	PAPER NUMBER

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

OK

Office Action Summary	Application No.	Applicant(s)	
	10/644,902	YIH ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 12 November 2004.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-13 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-10 and 12-13 is/are rejected.
 7) Claim(s) 11 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 12 November 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

1. Applicant's Amendment filed 11/12/2004 has been reviewed and placed of record in the file.
2. Applicant's arguments with respect to amended claims 1-10 and 12-13, filed 11/12/2004, have been considered but they are moot in view of new ground(s) of rejection.

Claim Objections

3. **Claim 2** is objected to because of the following informalities: Claim 2 recites: "wherein each of said plurality of isolation regions is shallow is shallow trench isolation" which should be "wherein each of said plurality of isolation regions is a shallow trench isolation region".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

- (e) the invention was described in
 - (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
 - (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-2, 4-7, 9-10, and 12-13** are rejected under 35 U.S.C. 102(e) as being anticipated by Song et al. U.S. Patent 6,635,532.

Song discloses in Figures 1 and 3's through 11's, particularly Figs. 1 and 11B, and respective portions of the specification a structure of nonvolatile memory array as claimed.

Referring to **claim 1**, Song discloses a structure of nonvolatile memory array, comprising:

a substrate (100, Fig. 11B);

a plurality of isolation regions (105, Figs. 1 and 11B) in said substrate;

a buried conductive region (113a, a source line buried into the substrate by impurity diffusion, column 5, lines 35-38) between said plurality of isolation regions, wherein said buried conductive region is perpendicular to each of said plurality of isolation regions (best seen in Fig. 1); and

a plurality of gate structures (WL, Fig. 1, 107/108/109, Fig. 11B) on said substrate except not on said buried conductive region (113a).

Referring to independent **claim 9** and dependent **claims 6 and 7**, and using the same reference characters and citations where applicable, Song discloses a structure of nonvolatile memory array, comprising:

a substrate;

a plurality of isolation regions in said substrate;

a plurality of gate structures on said substrate.

a buried source line (113a) between said plurality of isolation regions, wherein said buried source line is perpendicular to each of said plurality of isolation regions, and wherein the gate structures are not positioned on said buried source line; and

a plurality of drain regions (114, column 5, lines 62-65) in said substrate.

Regarding **claims 2 and 10**, although not explicitly termed, each of said plurality of isolation regions 105 is formed in a shallow trench 104, therefore each of said plurality of isolation regions is aptly called a shallow trench isolation region.

Regarding **claims 4 and 12**, Song further discloses that each of said plurality of gate structures (107/108/109) comprises at least a polysilicon layer (108, column 4, lines 49-55).

Referring to **claims 5 and 13**, Song further discloses a plurality of contacts (117) on said substrate.

5. **Claims 1-5 and 7-8** are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. U.S. Patent 6,211,012.

Lee discloses in Figs. 2's through 3, particularly Figs. 2F and 2H, and respective portions of the specification a structure of nonvolatile memory array as claimed.

Referring to **claim 1**, Lee discloses a structure of nonvolatile memory array, comprising:
a substrate (100, Fig. 2F);
a plurality of isolation regions (102) in said substrate;
a buried conductive region (such as the *center* "source region" 124 (column 3, lines 35-44), which is not visible from the figures, but best visualized from Fig. 2C) between said plurality of isolation regions, wherein said buried conductive region is perpendicular to each of said plurality of isolation regions; and
a plurality of gate structures (110) on said substrate except not on said buried conductive region (124).

Regarding **claim 2**, Lee further discloses that each of said plurality of isolation regions (102) is a shallow trench isolation region (column 3, first paragraph).

Referring to **claim 3**, best seen in Fig. 2C, a depth of drain region 122 is less than a depth of isolation regions 102; it follows that a depth of said buried conductive region 124, which is source region, which has, as is known in the art, the same characteristics as drain region 122, is less than a depth of each of said isolation regions 102.

Regarding **claim 4**, Lee further discloses that each of said plurality of gate structures (110) comprises at least a polysilicon layer (114, column 3, lines 14-17).

Referring to **claim 5**, Lee further discloses a plurality of contacts ("landing pads" 134) on said substrate.

Referring to **claim 7**, Lee further discloses a plurality of drain regions (122) in said substrate.

Referring to **claim 8**, Lee further discloses that said buried conductive region (124) is on a surface of said substrate, such that said buried conductive region is not under said plurality of isolation regions (102).

Allowable Subject Matter

6. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all

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limitations are considered within the claimed specific combination, fails to teach or render obvious a structure of nonvolatile memory array having **all** exclusive limitations as recited in claims 9 and 11, characterized in that a buried source line is between and is perpendicular to a plurality of isolation regions, gate structures are not positioned on said buried source line, and that a depth of said buried source line is less than a depth of said plurality of said isolation regions.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tu-Tu Ho
January 14, 2005



David Nelms
Supervisory Patent Examiner
Technology Center 2800